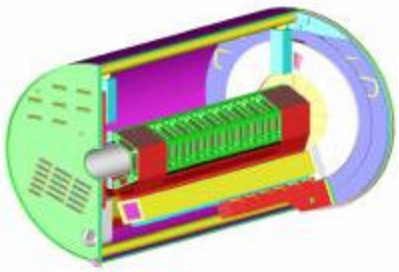


MVD Shutdown Plans/Needs

13-Feb-2002

John P. Sullivan

Why do we want the MVD?

Finding the vertex with sufficient precision necessary for several topics in p-p and p-A collisions (i.e. J/Psi - psiprime separation)

Unbiased centrality measurement

Determination of reaction plane

Two Main outstanding technical issues (and some minor ones too)

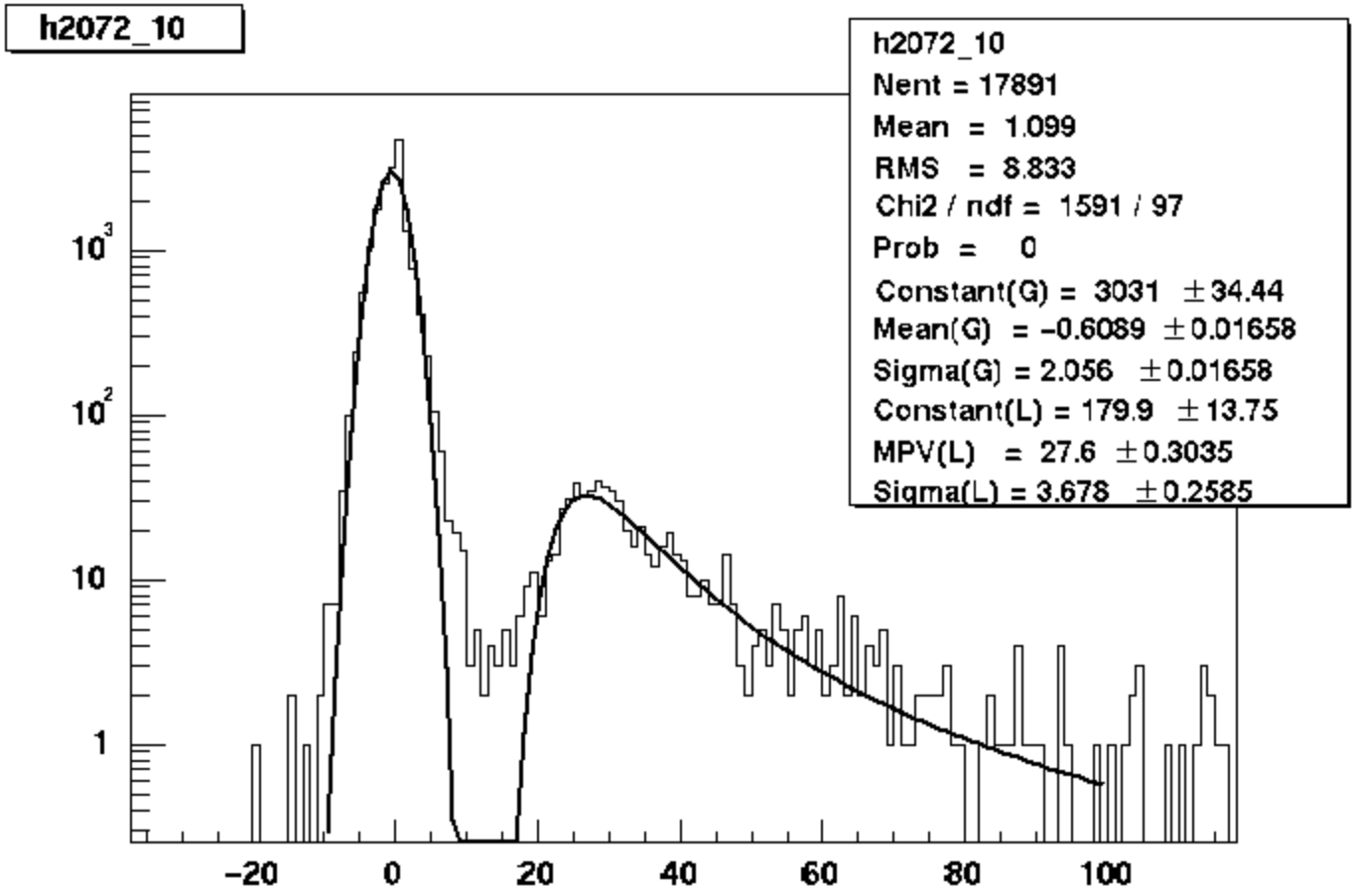
1) The majority of channels suffer from lower-than-expected signal size

2) wandering channel pedestals require frequent calibration

The main non-technical problem:

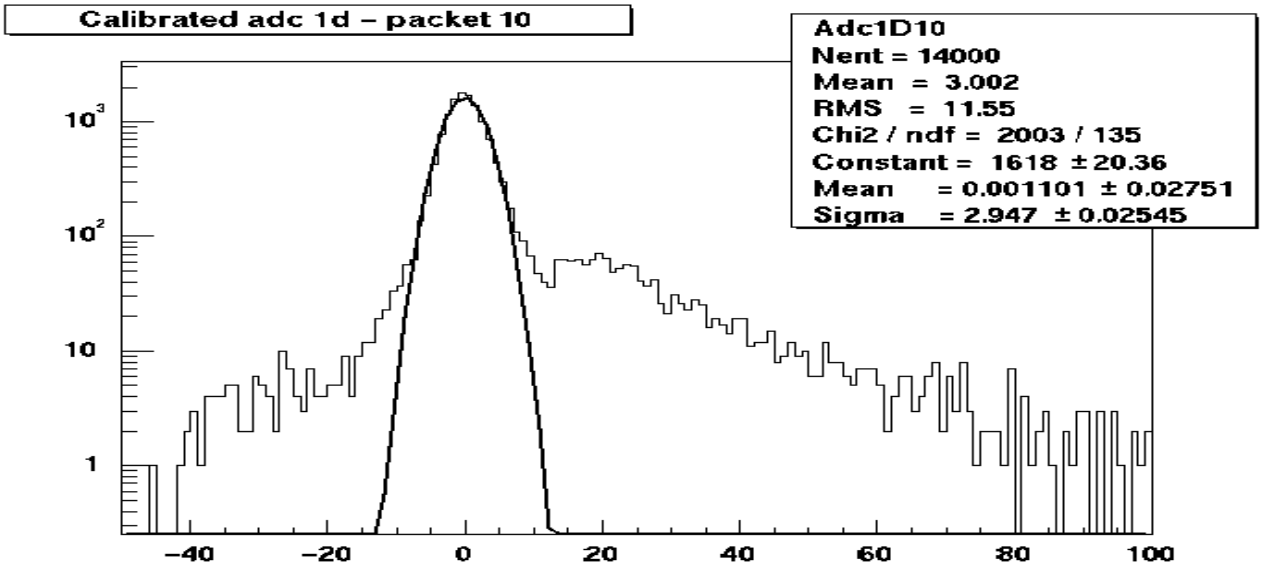
Hubert, Allan, and I cannot solve those problems without help

Calibrated signal for a pad detector

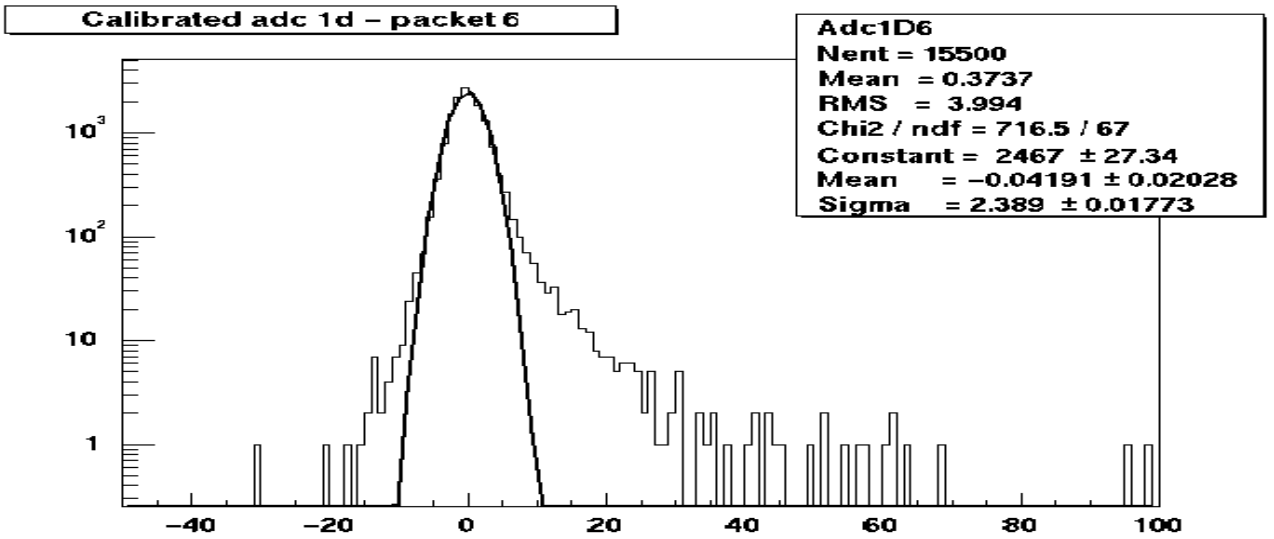


Good vs. “Poor” packet (1d)

Good:

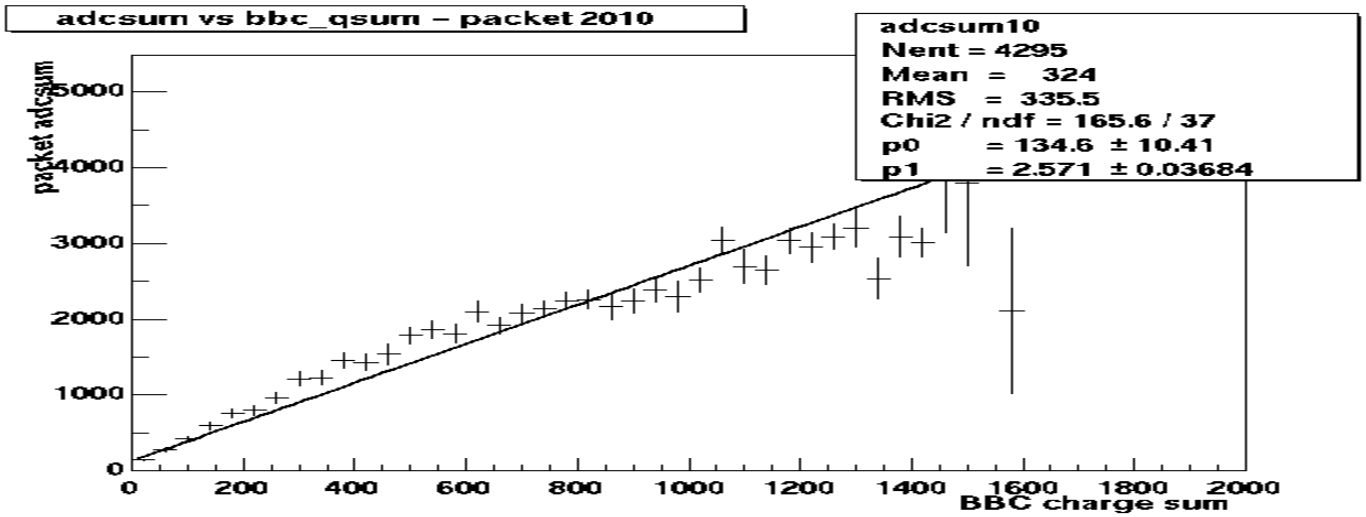


Poor:

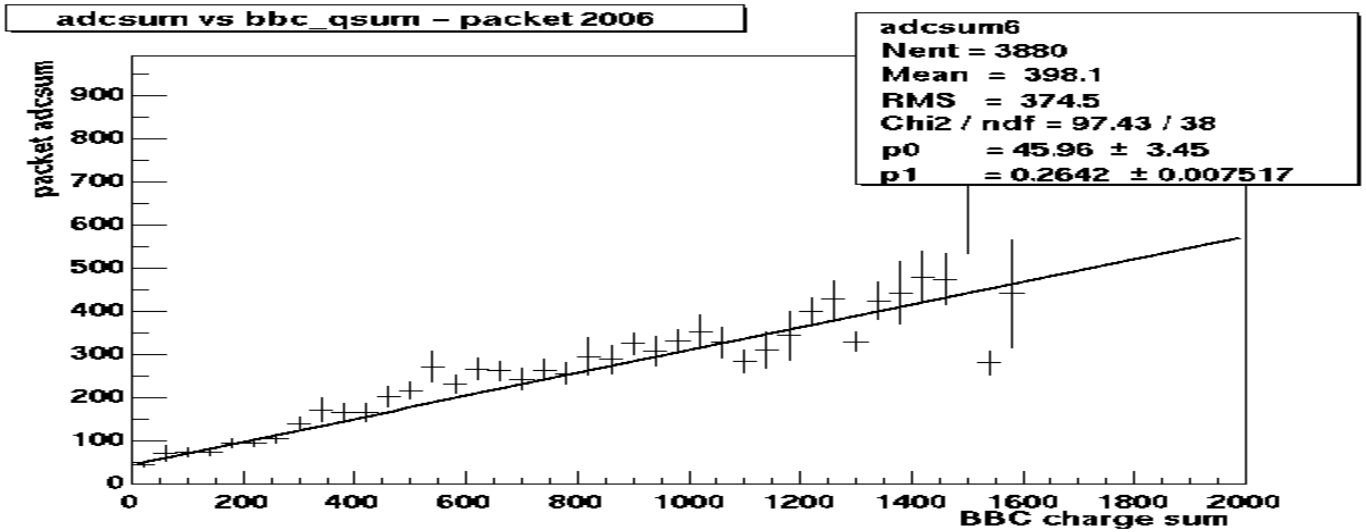


Packet ADC sum vs. BBC ADC sum

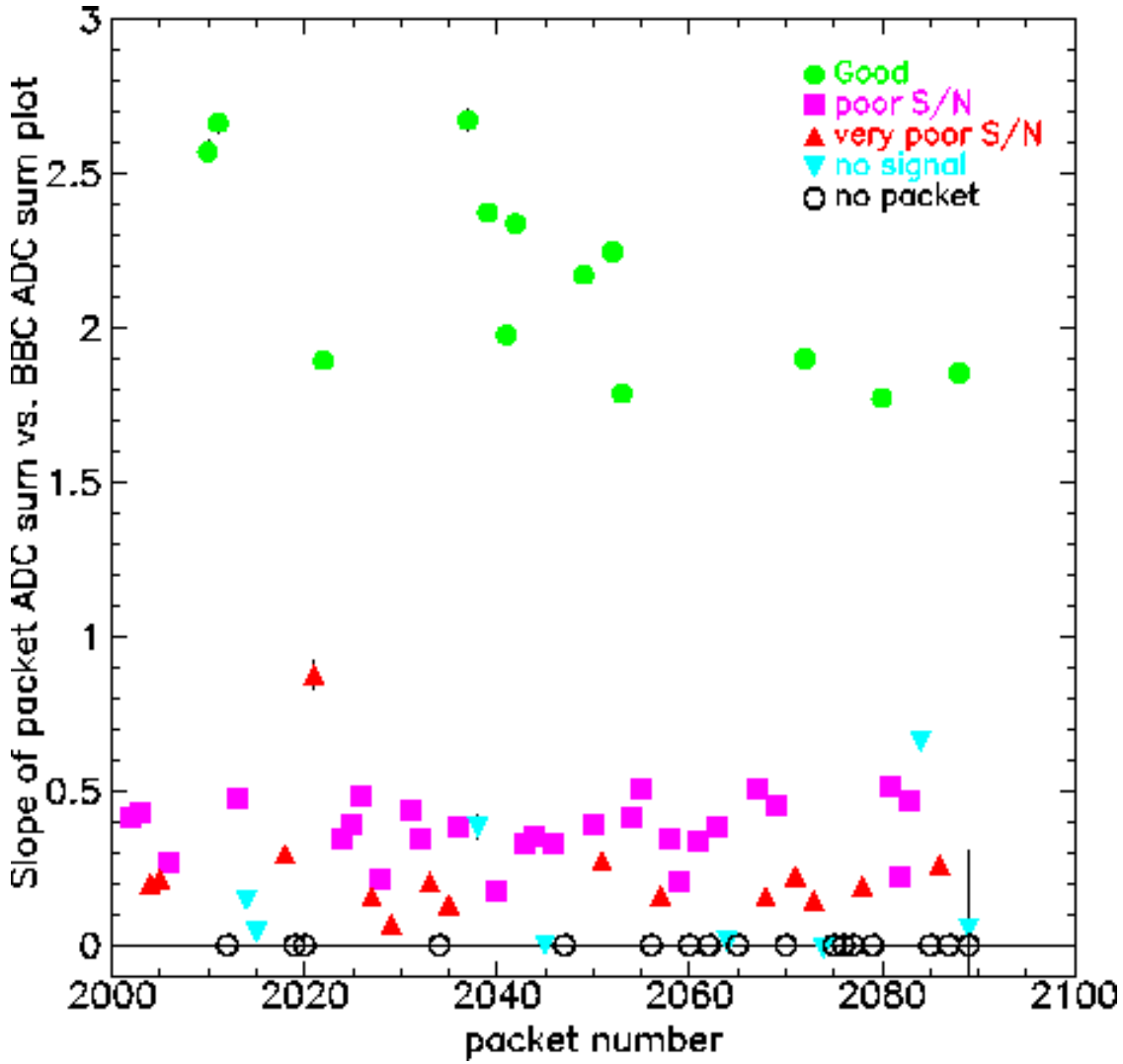
Good: slope= 2.57



Poor: slope= 0.26



Summary of “slope” vs. packet



What do we know about the poor signal/noise problem?

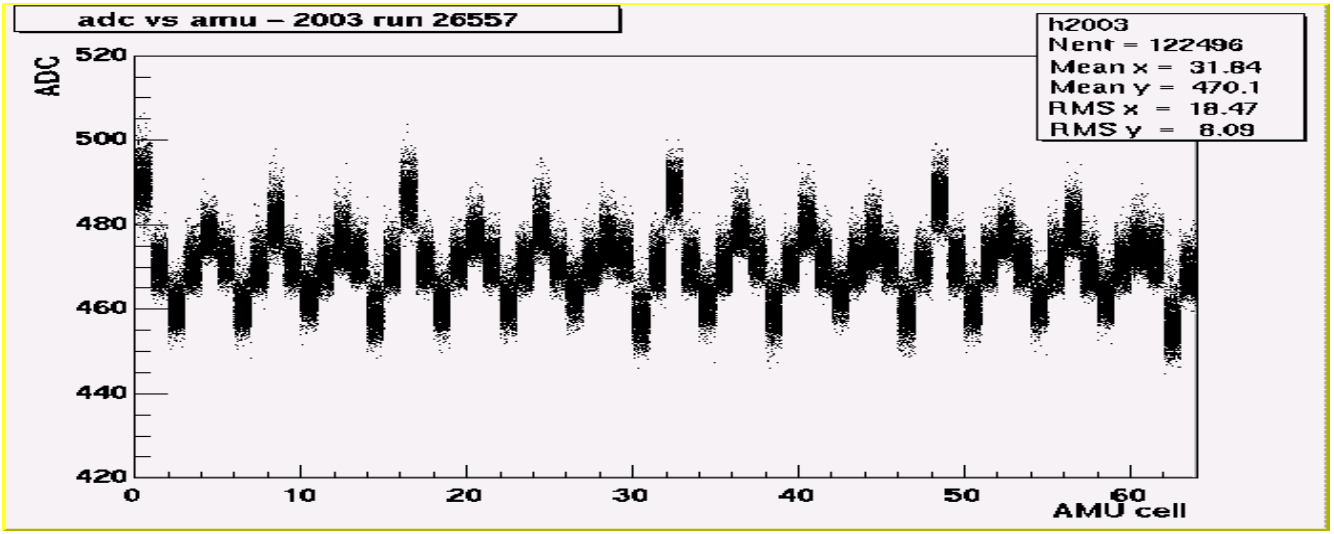
1) The problem is in the signal
2) It is intermittent in some packets

Possible causes:

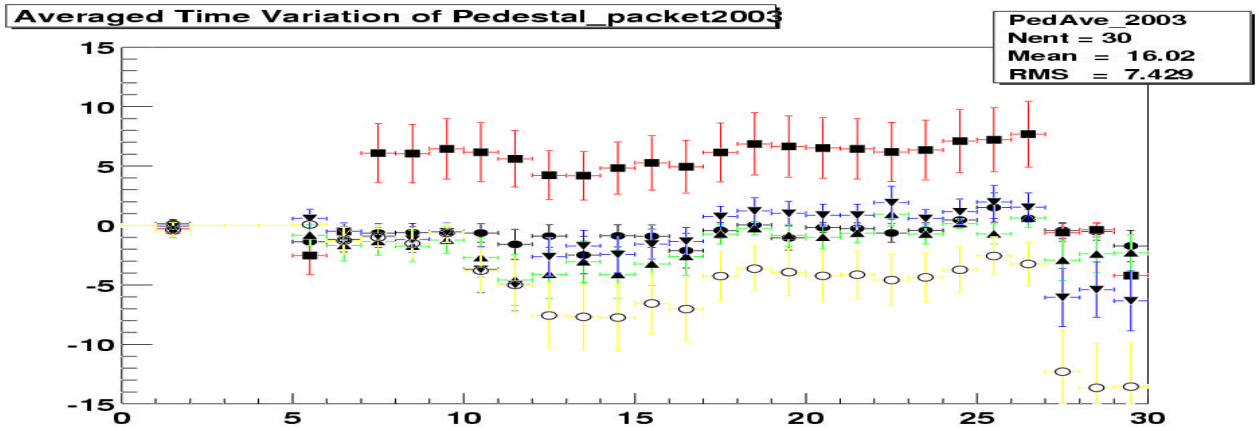
1) problem with bias voltage
2) level-1 timing wrong in some MCMs
3) preamplifiers "hit the rail" and are not reset often enough

Two Pedestal Problems

Pedestals depend on AMU cell #



Pedestals drift: (horizontal axis represents runs taken over ~10 days)



Both are problems for zero suppression.

AMU dependence -- What do we know?

The pedestal position depends on AMU cell number. The dependence varies with run number.

The AMU cell number dependence is seen in other subsystems (e.g. EMCAL), but at roughly 1/10 of this level.

We can calibrate the problem away (corrected in DCMs), but the algorithm is probably impractical in pipelined mode.

We are unsure of the time scale of the shifts, but it seems long -- we did calibrations to correct this once per day.

Pedestal drift -- What do we know?

We saw pedestal drift in Si+MCM system on the bench: ~15 chan/2.5 hours. Fastest shortly after turning the system on.

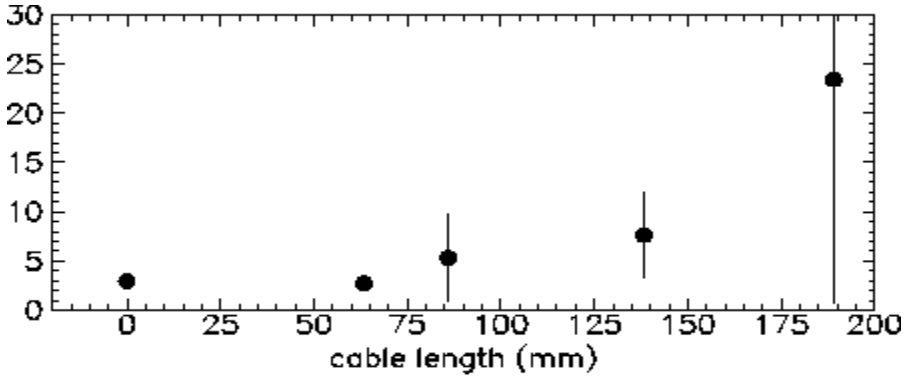
On bench, apparently no shift without Si detector attached.

There appear to be slow (~ hours) drift and more sudden shifts (<few minutes). Pedestals moved down ~25-50 channels when the beam was dumped in the PHENIX IR during an attempt to set level-1 timing. Pedestals slowly returned to original value after ~ 30 minutes.

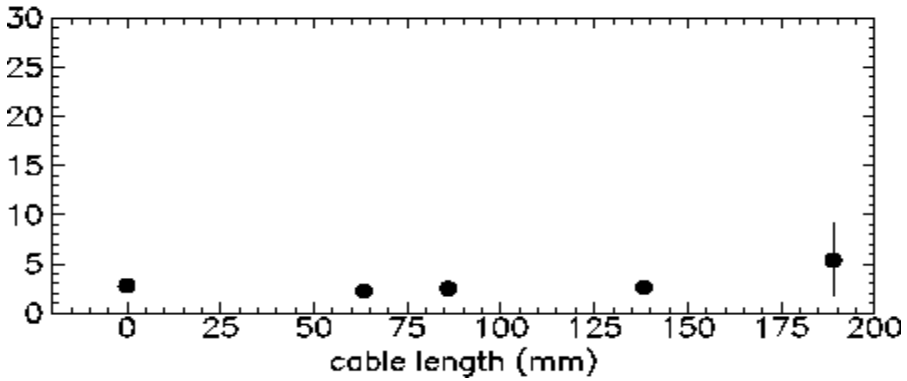
In the recent run, we did many calibrations to keep zero-suppression up-to-date. This annoys the shift crew.

Pedestal widths

The pedestal width depends on the length of the cable connecting the Silicon detector and the MCM:



Pedestal width before event-by-event correction (sigma in ADC chan)



Pedestal width after event-by-event correction

far → Close to beam pipe

What will we do about pedestal problems?

Add shielding around cables from detector to MCM -- should help with pedestal width at least.

More benchtop studies at LANL.

Tests with ~complete setup at BNL.

Steps needed to complete installation

Diagnosis and repair of problems in existing system: ~7 person months

Repair cooling tubes (not discussed): ~1/2 person month

Build and test additional detectors (not discussed): ~3.5 person months

Assemble, install, test completed system (not discussed): ~2 person months

Optional but important (not discussed): improve ease of operation: ~6 person months

Total: ~18 person months

Schedule

Estimated hardware effort ~18 person months.

We have ~8 months to do it.

Want to keep Allan on analysis full time.

We have max ~ 6 months of my time and ~ 8 months of Hubert's time.

We do not seem to have enough people to do the work.

Repair cooling tubes (continued)

The problem:
"Galvanic corrosion" where the brass fittings touched the Al tubes. Holes created when disconnecting the fittings.

The solution: Disassemble MVD, remove Al tubes, glue on Cu tubes. It is not conceptually hard. It will take ~2 person weeks to do this. In 1/1 previous tests, the tube came off the motherboard without problems.

Summary: We must fix this, but we know how.

Readout problems in DCIM boards

Problems which are probably simple to fix but hard to find (e.g. broken or shorted traces) prevented ~6/81 MCMs from being read out.

10/81 packets are returned with bad formats, these may also be easy to fix, but will take time to diagnose.

We used the best 20 out of 36 boards. We need 24 boards for the next run.

Guestimated time for this: 2 months for a person with electronics skills, patience, and good eyes.